Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (currently amended) A method for preventing regulated supply undershoot in state retained latches of a leakage controlled system, the method comprising the steps of:

providing a leakage control voltage source configured to supply a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system; and

biasing the voltage source via a reference voltage, wherein the reference voltage is provided via a charge storage device that is pre-charged to the active operation core voltage level when the system is in its active mode, such that when the system enters its sleep mode, the reference voltage slowly ~~discharges~~ decays to the sleep voltage level, and further such that when the system enters its sleep mode, the output of the voltage source goes through its transient phase and undershoots at a voltage level higher than the sleep voltage before finally settling to the sleep voltage level.

Claim 2. (currently amended) The method according to claim 1, wherein the step of providing a reference voltage via a ~~pre-charged~~ charge storage device comprises pre-charging a capacitor to the active operation core voltage level via a pre-charge switch.

Claim 3. (original) The method according to claim 1, wherein the voltage source comprises a low drop-out regulator.

Claim 4. (original) The method according to claim 1, wherein the voltage source comprises a linear regulator.

Claim 5. (original) The method according to claim 1, wherein the voltage source comprises a switched regulator.

Claim 6. (currently amended) A method for preventing regulated supply undershoot in state retained latches of a leakage controlled system, the method comprising the steps of:

providing means for supplying a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system; and

biasing the sleep voltage level supplying means via a reference voltage provided by a charge storage device that is pre-charged to the active operation core voltage level when the system is in its active mode, such that when the system enters its sleep mode, the reference voltage slowly ~~discharges~~ decays to the sleep voltage level, and further such that when the system enters its sleep mode, the output of the sleep voltage level supplying means goes through its transient phase and undershoots at a voltage level higher than the sleep voltage before finally settling to the sleep voltage level.

Claim 7. (currently amended) The method according to claim 6, wherein the step of biasing the sleep voltage level supplying means via a reference voltage provided by a ~~pre-charged~~ charge storage device comprises pre-charging a capacitor to the active operation core voltage level via a pre-charge switch.

Claim 8. (original) The method according to claim 6, wherein the means for supplying a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep

voltage is high enough to allow logic device state retention in the leakage controlled system, comprises a leakage control low drop-out regulator.

Claim 9. (original) The method according to claim 6, wherein the means for supplying a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system, comprises a leakage control voltage source.

Claim 10. (original) The method according to claim 9, wherein the voltage source comprises a low drop-out regulator.

Claim 11. (original) The method according to claim 9, wherein the voltage source comprises a linear regulator.

Claim 12. (original) The method according to claim 9, wherein the voltage source comprises a switched regulator.

Claim 13. (currently amended) A leakage control voltage source comprising ~~configured~~

a circuit to prevent regulated supply undershoot in a leakage controlled system and to supply a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system; and

when the leakage controlled system is operable to enter the sleep mode, the active operation core voltage level slowly decays to the sleep voltage level.

Claim 14. (currently amended) The leakage control voltage source according to claim 13, further comprising a charge storage device that is pre-charged to the active operation core voltage level when the leakage controlled system is in its

active mode, such that when the system enters it sleep mode, the charge storage device slowly discharges to the sleep voltage level, and the circuit further operable such that when the system enters it sleep mode, the output of the voltage source goes through its transient phase and undershoots at a voltage level higher than the sleep voltage before finally settling to the sleep voltage level.

Claim 15. (currently amended) The leakage control voltage source according to claim 13 ~~14~~, further comprising a pre-charge switch configured[s] to transfer a pre-charge to the charge storage device.[.]

Claim 16. (currently amended) The leakage control voltage source according to claim 13 ~~14~~, wherein the charge storage device comprises at least one capacitor.

Claim 17. (original) The leakage control voltage source according to claim 16, further comprising a pre-charge switch configured to transfer a pre-charge to the at least one capacitor.

Claim 18. (original) The leakage control voltage source according to claim 13, wherein the voltage source comprises a low drop-out regulator.

Claim 19. (original) The leakage control voltage source according to claim 13, wherein the voltage source comprises a linear regulator.

Claim 20. (original) The leakage control voltage source according to claim 13, wherein the voltage source comprises a switched regulator.

Claim 21. (currently amended) A leakage control voltage source operational in response to a reference voltage to prevent undesirable regulated supply undershoot in a leakage controlled system and to supply a sleep voltage level

below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system; and

wherein the reference voltage includes a decay that prevents the undesirable regulated supply undershoot.

Claim 22. (cancelled)

Claim 23. (original) The leakage control voltage source according to claim 21, further comprising a charge storage device that is pre-charged to the active operation core voltage level when the leakage controlled system is in its active mode, such that when the system enters its sleep mode, the charge storage device slowly discharges to the sleep voltage level, and further such that when the system enters its sleep mode, the output of the voltage source goes through its transient phase and undershoots at a voltage level higher than the sleep voltage before finally settling to the sleep voltage level.

Claim 24. (currently amended) The leakage control voltage source according to claim 21 ~~23~~, further comprising a pre-charge switch configured to transfer a pre-charge to the charge storage device.

Claim 25. (currently amended) The leakage control voltage source according to claim 21 ~~23~~, wherein the charge storage device comprises at least one capacitor.

Claim 26. (original) The leakage control voltage source according to claim 25, further comprising a pre-charge switch configured to transfer a pre-charge to the at least one capacitor.

Claim 27. (original) The leakage control voltage source according to claim 21, wherein the reference voltage is generated via a low drop-out regulator.

Claim 28. (original) The leakage control voltage source according to claim 21, wherein the reference voltage is generated via a linear regulator.

Claim 29. (original) The leakage control voltage source according to claim 21, wherein the reference voltage is generated via a switched regulator.

Claim 30. (new) A leakage control voltage source comprising

a circuit to prevent regulated supply undershoot in a leakage controlled system and to supply a sleep voltage level below an active operation core voltage level and above a predetermined minimum level during a sleep mode, such that the sleep voltage is high enough to allow logic device state retention in the leakage controlled system; and

the circuit comprising a charge storage device that is pre-charged to the active operation core voltage level when the leakage controlled system is in its active mode, such that when the system enters it sleep mode, the charge storage device slowly discharges to the sleep voltage level.